CLAIMS

1. An integrated circuit device, comprising:

a memory array including a plurality of word lines and a plurality of bit lines, and configured to support vertical pages, vertical pages including a plurality of byte wide sets of memory cells, the byte wide sets of memory cells being coupled to respective word lines in the plurality of word lines, and coupled to bit lines in the plurality of bit lines in common with the other byte wide sets of memory cells of the vertical page;

decoder circuitry coupled to the memory array, the decoder circuitry addressing one byte at a time by selecting one word line in the plurality of word lines, and the bit lines in common with the other byte wide sets of memory cells of the vertical page for erase processes; and

a controller coupled to the decoder circuitry to control erasing of at least one selected byte within a selected page stored in memory cells coupled to a selected one word line, the controller including circuitry to map data stored in memory cells coupled to word lines in the selected page other than the selected one word line, to apply erase potentials to memory cells storing the at least one selected byte, and after applying erase potentials to memory cells storing the at least one selected byte, to verify that the memory cells in the selected page other than the memory cells coupled to the selected one word line have maintained thresholds indicated by the mapping, and to apply program potentials to memory cells in the selected page that do not pass verify.

2. The integrated circuit device of claim 1, wherein the memory array includes

a plurality of sectors, the respective sectors including a plurality of blocks, the respective blocks including a plurality of programmable and erasable memory cells arranged in rows along the plurality of word lines, and in columns along the plurality of bit lines;

wherein the byte wide set of memory cells includes one memory cell from each block in the plurality of blocks, and wherein the bit lines in common with the other byte wide sets of memory cells of the vertical page include one selected bit line within each block in the set of blocks of the particular sector.

3. The integrated circuit device of claim 1, wherein said byte wide set of memory cells includes eight memory cells.

4. The integrated circuit device of claim 1, including temporary storage, and wherein the circuitry to map the memory cells coupled to word lines in the selected page other than the selected one word line includes logic to read data in the selected page, and to store addresses of memory cells having a programmed threshold level in the temporary storage.

5. The integrated circuit device of claim 1, including temporary storage comprising a plurality of word line flags, and the circuitry to map memory cells coupled to word lines in the selected page other than the selected one word line includes logic to read data in the selected page, and to set flags in the plurality of word line flags for word lines coupled to memory cells having a programmed threshold level in temporary storage.

6. The integrated circuit device of claim 1, including temporary storage, and wherein the circuitry to map memory cells coupled to word lines in the selected page other than the selected one word line includes logic to read data in the selected page, and to store read data in the temporary storage.

7. The integrated circuit device of claim 1, wherein the circuitry to map memory cells coupled to word lines in the selected page other than the selected one word line, executes after the circuitry applies erase potentials to the selected byte.

8. The integrated circuit device of claim 1, wherein the circuitry to map memory cells coupled to word lines in the selected page other than the selected one word line, executes before the circuitry applies erase potentials to the selected byte.

9. The integrated circuit device of claim 1, wherein said at least one selected byte consists of one byte.

10. The integrated circuit device of claim 1, wherein two columns of memory cells are coupled to each of said bit lines in the plurality of bit lines, and memory cells in the two columns coupled to a particular bit line on a particular word line are erased by the

erase potentials applied to the particular word line and the particular bit line, and wherein said at least one selected byte consists of two bytes and the vertical page is two bytes wide.

11. The integrated circuit device of claim 1, wherein said memory cells comprise charge programmable memory cells.

12. The integrated circuit device of claim 1, wherein said memory cells comprise NROM memory cells.

13. The integrated circuit device of claim 1, wherein said memory cells comprise floating gate memory cells.

14. The integrated circuit device of claim 1, wherein said controller comprises a state machine, and voltage supply circuits.

15. The integrated circuit device of claim 1, wherein said erase potentials comprise a negative voltage on a word line coupled to memory cells storing the selected byte and a positive voltage on the bit lines coupled to the memory cells storing the selected byte.

16. The integrated circuit device of claim 1, wherein the controller includes circuits to apply the erase potentials on a word line coupled to memory cells storing the selected byte and on the bit lines coupled to the memory cells storing the selected byte, and to apply erase inhibit potentials to other word lines in the plurality of word lines in the selected page.

17. The integrated circuit device of claim 1, wherein the controller includes circuits to apply the erase potentials on a word line coupled to memory cells storing the selected byte and on the bit lines coupled to the memory cells storing the selected byte, and to float to other bit lines in the plurality of bit lines not coupled to memory cells storing the selected byte.

18. A method for performing byte erase in a programmable and erasable memory array, the memory array including a plurality of programmable and erasable memory cells arranged in rows and columns, and having a plurality of word lines coupled to

memory cells along a row and a plurality of bit lines coupled to memory cells along a column configured to support vertical pages, vertical pages including a plurality of byte wide sets of memory cells, the byte wide sets of memory cells being coupled to respective word lines in the plurality of word lines, and coupled to bit lines in the plurality of bit lines in common with the other byte wide sets of memory cells of the vertical page, the method comprising:

addressing at least one selected byte at a time for erase processes in a selected vertical page by selecting one word line, and bit lines in the plurality of bit lines in common with the other byte wide sets of memory cells of the vertical page;

mapping data in memory cells coupled to word lines in the selected vertical page other than the selected one word line;

applying erase potentials to memory cells storing the at least one selected byte; and

after applying erase potentials to memory cells storing the at least one selected byte, verifying that memory cells coupled to word lines in the selected page other than the selected one word line have maintained thresholds indicated by the mapping, and applying program potentials to memory cells in the selected page that do not pass verify.

19. The method of claim 18, wherein the memory array includes

a plurality of sectors, the respective sectors including a plurality of blocks, the respective blocks including a plurality of programmable and erasable memory cells arranged in rows along the plurality of word lines, and in columns along the plurality of bit lines;

wherein the byte wide set of memory cells includes one memory cell from each block in the plurality of blocks, and wherein the bit lines in common with the other byte wide sets of memory cells of the vertical page include one selected bit line within each block in the set of blocks of the particular sector.

20. The method of claim 18, wherein said byte wide set of memory cells includes eight memory cells.

21. The method of claim 18, wherein the mapping of data in the memory cells coupled to word lines in the selected vertical page other than the selected one word line includes reading data in the selected page, and storing addresses of memory cells having a programmed threshold level in temporary storage.

22. The method of claim 18, wherein the mapping of data in the memory cells coupled to word lines in the selected vertical page other than the selected one word line includes reading data in the selected page, and setting flags in a plurality of word line flags for word lines coupled to memory cells having a programmed threshold level in temporary storage.

23. The method of claim 18, wherein the mapping of data in the memory cells coupled to word lines in the selected vertical page other than the selected one word line includes reading data in the selected page, and storing read data in temporary storage.

24. The method of claim 18, wherein the mapping of data in the memory cells coupled to word lines in the selected vertical page other than the selected one word line is executed after applying erase potentials to the selected byte.

25. The method of claim 18, wherein the mapping of data in the memory cells coupled to word lines in the selected vertical page other than the selected one word line is executed before applying erase potentials to the selected byte.

26. The method of claim 18, wherein said at least one selected byte consists of one byte.

27. The method of claim 18, wherein two columns of memory cells are coupled to each of said bit lines in the plurality of bit lines, and memory cells in the two columns coupled to a particular bit line on a particular word line are erased by the erase potentials applied to the particular word line and the particular bit line, and wherein said at least one selected byte consists of two bytes and the vertical page is two bytes wide.

28. The method of claim 18, wherein said memory cells comprise charge programmable memory cells.

29. The method of claim 18, wherein said memory cells comprise nitride MOS memory cells.

30. The method of claim 18, wherein said memory cells comprise floating gate memory cells.

31. The method of claim 18, wherein said erase potentials comprise a negative voltage on a word line coupled to memory cells storing the selected byte and a positive voltage on the bit lines coupled to the memory cells storing the selected byte.

32. The method of claim 18, wherein applying the erase potentials includes applying erase voltages on a word line coupled to memory cells storing the selected byte and on the bit lines coupled to the memory cells storing the selected byte, and applying erase inhibit potentials to other word lines in the plurality of word lines.

33. The method of claim 18, wherein applying the erase potentials includes applying erase voltages on a word line coupled to memory cells storing the selected byte and on the bit lines coupled to the memory cells storing the selected byte, and floating to other bit lines in the plurality of bit lines.